WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device, comprising:

forming a semiconductor layer;

forming a gate insulating film on the semiconductor film;

forming a first conductive layer over the gate insulating film;

forming a second conductive layer on the first conductive layer;

etching the first conductive layer and the second conductive layer to form a first conductive-layer pattern;

selectively etching the second conductive layer in the first conductive-layer pattern with plasma of boron trichloride, chlorine, and oxygen to form a second conductive-layer pattern; and

forming a first impurity region and a second impurity region in the semiconductor layer.

2. A method for manufacturing a semiconductor device, comprising:

forming a semiconductor layer;

forming a gate insulating film on the semiconductor film;

forming a first conductive layer over the gate insulating film;

forming a second conductive layer on the first conductive layer;

forming a third conductive layer on the second conductive layer;

etching the first conductive layer, the second conductive layer, and the third conductive layer to form a first conductive-layer pattern;

selectively etching the second conductive layer and the third conductive layer in the first conductive-layer pattern with plasma of boron trichloride, chlorine, and oxygen to form a second conductive-layer pattern; and

forming a first impurity region and a second impurity region in the semiconductor layer.

3. The method according to claim 1, wherein the first conductive-layer pattern is

formed to make an edge have a tapered shape.

4. The method according to claim 2, wherein the first conductive-layer pattern is formed to make an edge have a tapered shape.

5. The method according to claim 1, wherein the first conductive layer comprises tantalum nitride and the second conductive layer comprises one of titanium and an alloy or a compound containing titanium as its main component.

6. The method according to claim 2, wherein the first conductive layer comprises tantalum nitride and the second conductive layer comprises one of titanium and an alloy or a compound containing titanium as its main component.

7. The method according to claim 1, wherein the second conductive layer in the second conductive-layer pattern is formed to have an edge positioned inside an edge of the first conductive layer.

8. The method according to claim 2, wherein the second conductive layer and the third conductive layer in the second conductive-layer pattern are formed to have edges positioned inside an edge of the first conductive layer.

9. The method according to claim 1, wherein the semiconductor layer is doped with an impurity while using the second conductive-layer pattern as a mask to form the first impurity region and the second impurity region.

10. The method according to claim 2, wherein the semiconductor layer is doped with an impurity while using the second conductive-layer pattern as a mask to form the first impurity region and the second impurity region.

11. The method according to claim 1, wherein the second impurity region is

formed in a region overlapped with the first conductive layer in the second conductive-layer pattern.

12. The method according to claim 2, wherein the second impurity region is formed in a region overlapped with the first conductive layer in the second conductive-layer pattern.

13. A method for manufacturing a semiconductor device, comprising:

forming a semiconductor layer;

forming a gate insulating film on the semiconductor film;

forming a first conductive layer over the gate insulating film;

forming a second conductive layer on the first conductive layer;

etching the first conductive layer and the second conductive layer to form a first conductive-layer pattern;

selectively etching the second conductive layer in the first conductive-layer pattern with plasma of boron trichloride, chlorine, and oxygen to form a second conductive-layer pattern; and

doping the semiconductor layer with an impurity element through the first conductive layer in the second conductive-layer pattern to form an LDD region.

14. A method for manufacturing a semiconductor device, comprising:

forming a semiconductor layer;

forming a gate insulating film on the semiconductor film;

forming a first conductive layer over the gate insulating film;

forming a second conductive layer on the first conductive layer;

forming a third conductive layer on the second conductive layer;

etching the first conductive layer, the second conductive layer, and the third conductive layer to form a first conductive-layer pattern;

selectively etching the second conductive layer and the third conductive layer in the first conductive-layer pattern with plasma of boron trichloride,

chlorine, and oxygen to form a second conductive-layer pattern; and

doping the semiconductor layer with an impurity element through the first conductive layer in the second conductive-layer pattern to form an LDD region.

15. The method according to claim 13, wherein the first conductive-layer pattern is formed to make an edge have a tapered shape.

16. The method according to claim 14, wherein the first conductive-layer pattern is formed to make an edge have a tapered shape.

17. The method according to claim 13, wherein the first conductive layer comprises tantalum nitride and the second conductive layer comprises one of titanium and an alloy or a compound containing titanium as its main component.

18. The method according to claim 14, wherein the first conductive layer comprises tantalum nitride and the second conductive layer comprises one of titanium and an alloy or a compound containing titanium as its main component.

19. The method according to claim 13, wherein the second conductive layer in the second conductive-layer pattern is formed to have an edge positioned inside an edge of the first conductive layer.

20. The method according to claim 14, wherein the second conductive layer and the third conductive layer in the second conductive-layer pattern are formed to have edges positioned inside an edge of the first conductive layer.